

# Controlled Erasure as a Building Block for Universal Thermodynamically-Robust Superconducting Computing

Christian Z. Pratt,<sup>\*</sup> Kyle J. Ray,<sup>†</sup> and James P. Crutchfield<sup>‡</sup>  
*Complexity Sciences Center and Department of Physics and Astronomy,  
 University of California, Davis, One Shields Avenue, Davis, CA 95616*  
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Reducing the energy inefficiency of conventional CMOS-based computing devices—which rely on logically irreversible gates to process information—remains both a fundamental engineering challenge and a practical social challenge of increasing importance. In this work, we extend an alternative computing paradigm which utilizes distributions of microstates to store information in the metastable minima determined by an effective potential energy landscape. These minima serve as mesoscopic memory states which are manipulated by a dynamic landscape to perform information processing. Central to our results is the *control erase* (CE) protocol, which manipulates the landscape’s metastable minima to control whether information is preserved or erased. Importantly, successive executions of this protocol can implement a NAND gate—a logically-irreversible universal logic gate. We show how to practically implement this in a device created by two inductively coupled superconducting quantum interference devices (SQUIDs). We identify circuit parameter ranges that give rise to effective CEs and characterize the protocol’s robustness by comparing relevant protocol timescales. Due to their superconducting operational temperatures, performing optimized CEs with SQUIDs can serve as a platform for highly energy-efficient universal computation.

## I. INTRODUCTION

Conventional classical computing systems harness irreversible logic gates—e.g., NAND gates—to process information. Irreversibility arises from erasing input information to create desired output states, coming at a minimum theoretical heat dissipation cost of  $k_B T \ln 2$  [1] per erasure. During their operation, current conventional CMOS-based computational devices generate  $\mathcal{O}(10^4)$  times more heat than this minimum cost [2–5]. On the social scale, energy consumption for computational purposes is projected to reach 20% of global energy demand by 2030 [6]. In light of this, it is time to investigate alternative strategies and substrates that give rise to energy-efficient universal computation.

One strategy implied in Landauer’s seminal 1961 result [1, 7–14] focuses on manipulating metastable energy minima in an effective potential energy landscape. Coarse-graining the microstate phase-space surrounding the minima yields long-lived mesoscopic memory states that correspond to the logical 0s and 1s for binary computation. From this perspective, a computation is implemented by controlling memory-state dynamics by changing the potential energy landscape. A computation is then a map between initial and final memory states. This “energy first” perspective of computation allows for careful analysis and prediction of a given logic gate’s performance and efficiency [1, 7, 11, 14].

Elaborating on this framework, Sec. II first describes the characteristics of a potential energy landscape capable of storing two bits of information. Sec. III introduces a family of *control erase* (CE) protocols—two-dimensional generalizations of single-bit erasure protocols. Sec. IV then presents a device constructed from two inductively coupled superconducting quantum interference devices (SQUIDs) [15–20]. This device implements

the required potential energy landscape and executes CE protocols by changing its circuit parameters. Sections V A–V C characterize the effectiveness of the SQUID CE implementation by exploring circuit parameter ranges. Notably, with serial executions of CEs, a robust NAND gate can be performed, as detailed in Sec. V D. Executing robust NAND gates with this device could lead to extremely low energy universal computations.

## II. PHYSICAL COMPUTING VIA METASTABLE LANDSCAPES

We assume a potential energy landscape of interest supports several energy minima and an underlying physical substrate, which is connected to a thermal environment that introduces damping and noise into its dynamics. The minima are separated by energy barriers substantially larger than the thermal energy  $k_B T$ . The thermal environment quickly induces distributions of microstates to settle into local equilibria in the phase-space regions surrounding the minima. Noise, though, perturbs the microstates within their respective regions. However, it is unlikely to drive the microstates between these regions on a timescale that is exponential in energy barrier height. The energy barriers prevent mixing between these regions except on these very long timescales; as a result, the minima serve to support long-lived mesoscopic system states—metastable memory states. Manipulating them with the potential’s dynamics corresponds to information processing.

The following details physically-embedded computations via landscape control [1, 13, 21–24]. Specifically, these computations are stochastic mappings from the set of initial to final memory states  $\mathcal{M}$ . Here, we introduce the *control erase* (CE) protocol over two input bits. One

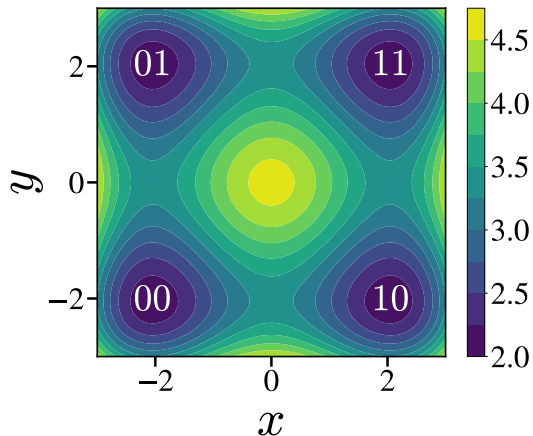


FIG. 1. Example 2-bit memory mesoscopic-state instantiation: Regions surrounding energy minima provide metastable information storage, whose bit value is assigned according to Eq. (1). Controlling this energy landscape manipulates the memory state’s dynamics—implementing information processing.

way of embedding 2-bit computations is to control a two-dimensional potential with a minimum in each quadrant. The memory states are distinguished using the  $x$  and  $y$  axes:

$$\text{first [second] bit} = \begin{cases} 0 & \text{if } x [y] < 0, \\ 1 & \text{if } x [y] > 0. \end{cases} \quad (1)$$

Fig. 1 illustrates a quadruple-well potential with an example memory-state instantiation chosen by the locations of the minima according to Eq. (1). The computational operations to be performed on the potential—i.e., the deterministic transformation of the potential that maps information from initial to final metastable memory states—are referred to as a *physical protocol*.

Last, we formally define metastable memory states in the  $x$ - $y$  plane and how they evolve under a computational protocol. Over the time interval  $t \in [t_i, t_f]$  and given an initial two-bit metastable memory state  $(\mathbf{X}, \mathbf{Y}) := (m_x(t = t_i), m_y(t = t_i)) \in \mathcal{M}$ , the final memory state  $(\mathbf{X}', \mathbf{Y}') := (m_x(t = t_f), m_y(t = t_f))$  is determined by the conditional probability  $\mathbf{p} = \Pr((\mathbf{X}', \mathbf{Y}') | (\mathbf{X}, \mathbf{Y}))$ . With this, the final microstate distribution  $\vec{p}(t = t_f)$  is updated through  $\vec{p}(t = t_f) = \mathbf{p} \vec{p}(t = t_i)$ . A deterministic logic gate is successfully performed when these conditional probabilities are very close to either 0 or 1.

### III. CONTROL ERASE PROTOCOL

The NAND gate is a binary logical gate that takes in two input bits, meaning there are four possible input states: 00, 01, 10, and 11—and outputs one bit—either 0 or 1. Specifically, the output state is 1 for all input

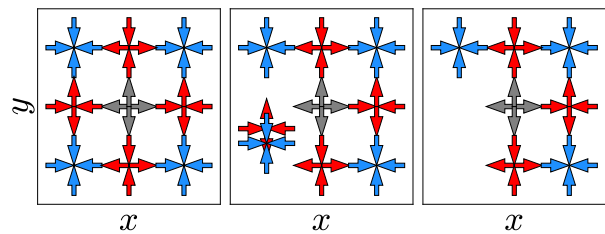


FIG. 2. Illustrating the control erase (CE) protocol via the “dynamical skeleton” of the potential energy landscape in Fig. 1, which only shows the potential’s fixed points and corresponding flow fields. Here, stable minima (unstable saddle) fixed points are colored blue (red), while grey indicates a local maximum. This CE is executed with respect to the  $y$  axis: The states contained on the negative  $x$  half plane undergo an erasure of  $Y$  to the 1 state, while those on the positive  $x$  half plane do not change. This results in the third quadrant’s stored information being erased into the second quadrant. **(Left)** Initial potential energy landscape configuration. **(Center)** The stable and unstable fixed points in quadrant III approach each other just before annihilation. **(Right)** Just after fixed point annihilation in the third quadrant, the most important step of this example CE. If this landscape is held long enough, all information initially stored in quadrant III will be erased to quadrant II. Importantly, all other fixed points are maintained during this time. One completes the CE protocol cycle by bringing the potential back to its starting configuration.

states except if both input bits are 1, in which case the output is 0. Now, consider having no knowledge of a NAND gate’s input state and subsequently reading the output state to be 1. Attempting to infer which specific two-bit input state led to this output state is impossible, as there are three possible input states that result in 1. Microscopically, a state-space contraction occurred during the NAND gates operation, and this manifested as an irreversible erasure of information. However, if the output was 0, then the input is trivially known to be 11. This is the underlying information processing task of the NAND gate: to preserve some input information, while erasing the rest. Thus, performing a NAND gate requires the ability to carry out controlled erasure protocols over the space of memory states.

Erasure protocols in one-dimensional systems have been studied previously [1, 11, 13, 25–29]. The following extends this to an erasure protocol via the two-dimensional potential shown in Fig. 1. The additional freedom given by the second dimension permits control over what information is preserved and erased. Via that control, a NAND operation can be performed. To accomplish this, we introduce the *control erase* (CE) protocol. Fig. 2 illustrates a CE protocol via the potential’s *skeleton*, which views the potential from a dynamical systems perspective—i.e., its fixed points and flow fields in the microscopic state space. In this example, the negative  $x$  half-plane executes an erasure protocol, while the positive  $x$  half-plane remains unchanged.

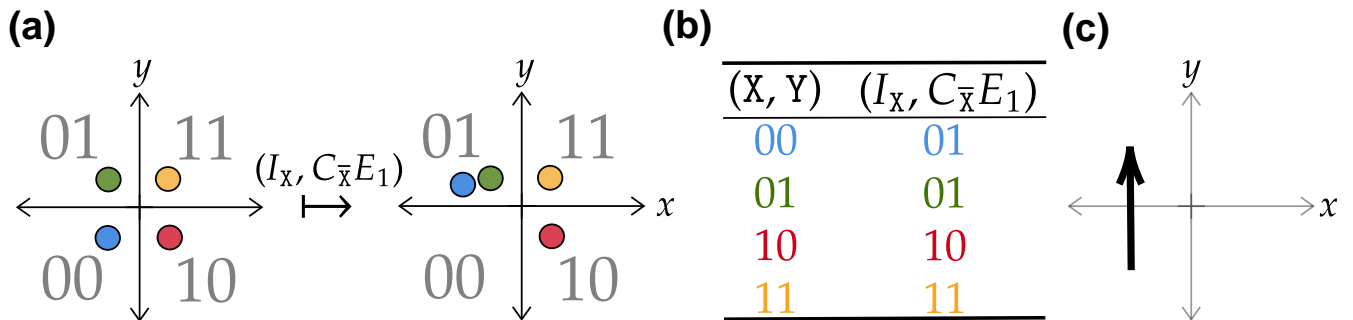


FIG. 3. **(a)** State mapping executed by the control erasure  $(\mathbf{x}', \mathbf{y}') = (I_X, C_{\bar{X}}E_1)$ . Each quadrant contains a coarse-grained metastable memory state, defined by Eq. (1). Every circle represents a distribution of microstates, i.e. information, and is colored based on its original memory-state instantiation. **(b)** CE truth table. The overline above state  $\mathbf{X}$ , in the symbol  $C_{\bar{X}}$ , indicates controlling on the negation of  $\mathbf{X}$ , erasing  $\mathbf{Y}$  to 1 only when  $\mathbf{X} = 0$ . **(c)** Arrow-based notation illustrating the  $(I_X, C_{\bar{X}}E_1)$  CE protocol. This depiction is also used in Sec. VD. Fig. 8 shows all CEs of interest.

Executing a given CE protocol requires three binary choices, illustrated via examples:

1. First, choose which of the two input bits to operate on. For example, erasing information only along the  $y$  axis requires operating only on the second bit so that  $\mathbf{Y}' \neq \mathbf{Y}$ . This implies that the first input bit is preserved, i.e.,  $\mathbf{X}' = \mathbf{X}$ . However, this does not fully specify the pair of states that involved in the CE: 00 and 01, or 10 and 11, are both candidate pairs for a  $\mathbf{Y}' \neq \mathbf{Y}$  operation.
2. Next, specify which pair of two-bit memory states are involved in the erasure. Suppose we select states 10 and 11. Doing this *controls* the erasure operation on  $\mathbf{X}$  such that it erases the information in  $\mathbf{Y}$  only if  $\mathbf{X} = 1$ . Otherwise, if  $\mathbf{X} = 0$ , then the information stored in  $\mathbf{Y}$  is preserved. This control will be denoted as  $C_X$ .
3. Finally, we choose whether  $\mathbf{Y}$  is erased to the 0 or the 1 state. This is denoted as  $E_1$ , for example, if we erase to the state 1;

These three binary choices produce eight CE protocols of interest; which are detailed in Fig. 8. We denote the particular choices in the examples above with  $\mathbf{Y}' = C_X E_1(\mathbf{X})$  and  $\mathbf{X}' = I_X(\mathbf{X})$ , where  $I_X$  indicates an identity operation of the  $\mathbf{X}$  input bit, since the information from the first bit  $\mathbf{X}$  is preserved. With this notation, and dropping the initial memory state dependence in the operations, the described CE protocol is written as:  $(\mathbf{x}', \mathbf{y}') = (I_X, C_X E_1)$ .

Fig. 3 shows multiple representations of another CE:  $(I_X, C_{\bar{X}}E_1)$ . We are still erasing information stored in  $\mathbf{Y}$ , but instead of erasing the information if  $\mathbf{X} = 1$ , the erasure happens if  $\mathbf{X} = 0$ . In other words, our control is  $\bar{\mathbf{X}}$  (NOT  $\mathbf{X}$ ), rather than  $\mathbf{X}$ . Of particular importance is the arrow-based notation in Fig. 3, which will be employed when detailing the NAND gate in Sec. VD.

Finally, to generalize the CE notation, first we know that one of the two output states  $\rho' \in \{\mathbf{X}', \mathbf{Y}'\}$  is created by the identity operation  $\rho' = I_\rho$ , where  $\rho \in \{\mathbf{X}, \mathbf{Y}\}$ . The other output state is created by  $C_\sigma E_A$ : Here,  $\sigma \in \{\rho, \bar{\rho}\}$  indicates the control state for an erasure to the  $A \in \{0, 1\}$  state. Note that the overline  $\bar{\rho}$  above  $\rho$  indicates a negation of the  $\rho$  state.

#### IV. DEVICE IMPLEMENTATION

In this work, superconducting quantum interference devices (SQUIDs) are employed as a physical platform for performing CE protocols. We first briefly review relevant superconducting device literature. Then, we specify the device of interest—two inductively coupled SQUIDs (SQUIDs), shown in Fig. 4—whose potential energy landscape can dynamically execute CE protocols.

The *quantum flux parametron* (QFP) was invented by Goto in 1985 [15, 30], whose primary focus was for energy-efficient classical computing applications in the superconducting regime. With the incentive of optimizing circuit parameters and operating on slower computational timescales to aid in energy efficiency, Takeuchi et al. introduced the *adiabatic QFP* [4, 31]. In contrast to our work, circuit parameters are not optimized via algorithms for thermodynamic performance, but are instead found by utilizing bifurcation theory. With a similar design construction as the QFP, but having the same equations of motion as the QFP, in 1989 Han et al. introduced the *variable  $\beta$  radio frequency SQUID* [16–18]. This device was later named the *compound Josephson junction radio frequency SQUID* (CJJ rf SQUID) [19, 32, 33]. Its principle use was for investigating macroscopic quantum phenomena (MQP). The goal of the present effort—demonstrating universal classical information and storage—is not shared with the CJJ rf SQUID literature.

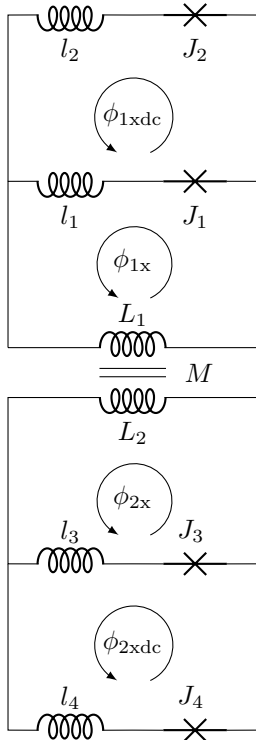


FIG. 4. Two inductively coupled SQUIDs interacting via mutual inductance coupling constant  $M$ .

This said, the circuit parameter values from these areas of literature is used in Sec. VC for evaluating the performance of the device of interest when performing CE protocols. Since QFPs and CJJ rf SQUIDs are both SQUIDs, we refer to the device in Fig. 4 as two inductively coupled SQUIDs. Ref. [20] introduced and detailed the device in Fig. 4. Importantly, it supports a potential equivalent to that of Fig. 1. To understand how it executes computations, the following gives a synopsis of the device's potential energy landscape created. Physically-grounded approximations and assumptions for executing a CE protocol are then detailed.

Fig. 4 illustrates a device consisting of two inductively coupled SQUIDs. In this circuit,  $L_i$  [ $l_j$ ] indicate the radio frequency [direct current] SQUID inductances, while  $J_j$  indicate Josephson junctions, all for which  $i = 1, 2$ , and  $j = 1, 2, 3, 4$ . This device generates the following potential energy surface:

$$\begin{aligned}
 U' = U/U_0 = & \frac{1}{2}(\varphi_1 - \varphi_{1x})^2 + \frac{1}{2}(\varphi_2 - \varphi_{2x})^2 \\
 & + \frac{\gamma_1}{2}(\varphi_{1dc} - \varphi_{1xdc})^2 + \frac{\gamma_2}{2}(\varphi_{2dc} - \varphi_{2xdc})^2 \\
 & - \beta_1 \cos \frac{\varphi_{1dc}}{2} \cos \varphi_1 - \beta_2 \cos \frac{\varphi_{2dc}}{2} \cos \varphi_2 \\
 & + \delta\beta_1 \sin \frac{\varphi_{1dc}}{2} \sin \varphi_1 + \delta\beta_2 \sin \frac{\varphi_{2dc}}{2} \sin \varphi_2 \\
 & + \mu(\varphi_1 - \varphi_{1x})(\varphi_2 - \varphi_{2x}). \quad (2)
 \end{aligned}$$

Here,  $U_0 = (\Phi_0/2\pi)^2/L_\alpha$ , where  $\Phi_0$  is the flux quantum,  $\varphi_r = (2\pi\phi_r)/\Phi_0$  is the reduced flux variable of the  $r$ th flux variable, and  $L_\alpha = \alpha L$  for which  $\alpha = 1 - M^2/L^2$  with  $M$  being a tunable mutual inductance between the two SQUIDs. Next,  $L := L_1 \approx L_2$ ,  $\gamma_i = L_\alpha/2l_i$  in which  $l_{1(2)} := l_{1(3)} \approx l_{2(4)}$ ,  $\beta_n = 2\pi L_\alpha(I_{c2(4)} + I_{c1(3)})/\Phi_0$ , and  $\delta\beta_n = 2\pi L_\alpha(I_{c2(4)} - I_{c1(3)})/\Phi_0$ , where each  $I_{cj}$  corresponds to the critical current  $I_c$  of the  $j$ th Josephson junction, with  $n = 1, 2$ . Lastly,  $\mu = M/L$ . Here,  $M$  is treated as a tunable constant: While its experimental implementation—a SQUID coupler—are discussed in Refs. [32–34], the coupler's dynamics will not be addressed here.

Note that Eq. (2) contains four degrees of freedom, namely  $\varphi_i$  and  $\varphi_{idc}$ , where  $i = 1, 2$ . This type of compound SQUID is generally constructed with  $\gamma \gg 1$  [18, 35]. This implies that any changes in  $\varphi_{ixdc}$  are rapidly observed in  $\varphi_{idc}$ , so we assume  $\varphi_{idc} = \varphi_{ixdc}$ . Applying this approximation to Eq. (2) projects the potential onto two dimensions, providing the potential energy surface shown in Fig. 1 in the  $\varphi_1$ - $\varphi_2$  plane.

Next, we assume that the fabrication consistency of the JJ elements is such that  $\delta\beta_1 = \delta\beta_2 = 0$ . In practice,  $\delta\beta_1 \neq \delta\beta_2 \neq 0$ , which results in a slight offset in the minima's locations [27]. This induced asymmetry in a real device can be at least partially compensated by external flux parameters if necessary. The  $\delta\beta = 0$  assumption is fairly common, and is made in order to streamline the process of analyzing the device's equation of motion. As a similar assumption, we let  $\beta := \beta_1 = \beta_2$  and, furthermore,  $I_c := I_{c1} = I_{c2} = I_{c3} = I_{c4}$ .

Finally, assuming small-valued coupling ratios, we drop terms that are quadratic in  $\mu$ , which yields  $\alpha \rightarrow 1$  and  $L_\alpha \rightarrow L$ .

All this done, rewriting Eq. (2) then gives:

$$\begin{aligned}
 U' = & \frac{1}{2}(\varphi_1 - \varphi_{1x})^2 + \frac{1}{2}(\varphi_2 - \varphi_{2x})^2 \\
 & - \beta \cos \frac{\varphi_{1xdc}}{2} \cos \varphi_1 - \beta \cos \frac{\varphi_{2xdc}}{2} \cos \varphi_2 \\
 & + \mu(\varphi_1 - \varphi_{1x})(\varphi_2 - \varphi_{2x}). \quad (3)
 \end{aligned}$$

Eq. (3) describes a dimensionless potential  $U'$  with two degrees of freedom; this will be frequently referred to for the remainder of this work. We manipulate this potential energy landscape with the following circuit parameters for  $i = 1, 2$ : (i)  $\varphi_{ix}$  tilts the potential with respect to the  $i$ th axis, (ii)  $\varphi_{ixdc}$  provides an in-situ barrier control on the  $i$ th axis, and (iii)  $\mu$  supplies a coupling interaction between the two circuits, which biases the potential to favor wells that lie on one of the two diagonals in the  $\varphi_1$ - $\varphi_2$  plane.

## V. CONTROL ERASE PROTOCOL IMPLEMENTATION

The approximations in Sec. IV yield the potential given in Eq. (3), and is displayed in Fig. 1. Manip-

ulating the aforementioned external circuit parameters implements any of the eight possible control erase (CE) protocols shown in Fig. 8. Using the CE  $(I_x, C_{\bar{x}}E_1)$  from Figs. 2 and 3 as an example, we detail how to find circuit parameter values that give rise to “effective” protocols in Sec. V A. We qualitatively show this by exploring circuit parameter values that give rise to ranges for which this particular CE can be executed. Furthermore, we quantify this protocol’s effectiveness—i.e., if it is highly robustness—in Sec. V C. Sec. V B generalizes to determine which circuit parameters will be used to carry out any CE protocol in Fig. 8. With this, Sec. V D demonstrates the physical execution of an effective NAND gate.

### A. Effective CE Protocol

Fig. 5 highlights the important fixed points on the potential immediately before and after the stable (red) and unstable (green) fixed points annihilate in the negative- $x$  half plane. After the annihilation, a CE is possible since the orange, blue, and purple fixed points on the positive- $x$  half plane are preserved. From the perspective detailed in Sec. III, the information stored in the Y state on the negative- $x$  half plane is erased, while all other information in the potential’s memory states is preserved. In this example,  $\Delta U'_{00}$  denotes the potential barrier required to vanish for the CE to be carried out. Once this barrier vanishes,  $\Delta U'_{01}$ ,  $\Delta U'_{10}$  and  $\Delta U'_{11}$  indicate the barriers that need to be maintained. The goal is to find the circuit parameter values which give these barriers sufficiently large heights, as this further contributes to a successful CE.

Fig. 5 illustrates bifurcation diagrams of the  $\varphi_2$  coordinate over a given circuit parameter range, while all other parameters are held constant. Motivated by Ozfidan et al. [36], we take  $\beta = 2.3$ . Additionally, the coordinate  $\varphi_2$  is solely illustrated because  $\varphi_1$  varies negligibly in comparison.

To guide exploring viable parameter values, a general view of the relationship between the dimensionless barrier heights illustrated in Fig. 5 and the energy scale of thermal fluctuations  $k_B T$  is useful. Understanding this aids in determining if a barrier height is energetically large enough to store microstates within a metastable memory state; for example, for the barrier to be no smaller than  $50 k_B T$ . At  $T = 100$  mK, this minimum requirement corresponds to a dimensionless barrier height of  $\Delta U' = 50 k_B T / U_0 = 0.15$  when using the circuit parameters of Ref. [36]. We indicate this barrier height with the dotted horizontal line in the insets of Fig. 5. This line will represent a proxy for characterizing dimensionless barrier heights. That is, if a circuit parameter’s value results in either  $\Delta U'_{01}$ ,  $\Delta U'_{10}$ , or  $\Delta U'_{11}$  falling below this line, then we say it is no longer able to reliably store information in the relevant well at 100 mK. Of course, this all varies based on the operating temperature and the circuit parameters, but this same process

can be carried out for any particular set of temperature and parameters.

The following now describes the qualitative consequences of changing each circuit parameter and the resulting potential in Fig. 5. First, as  $\mu$  increases, the depth of the minima representing the states 01 and 10 increases. Meanwhile, the minima depths in the 11 state decrease, leading to  $\Delta U'_{11}$  decreasing. This indicates that  $\mu$  should not take on too large of a value in order to avoid fluctuations over the  $\Delta U'_{11}$  barrier. Next, if the magnitude of  $\varphi_{2\text{xdc}}$  increases, then both  $\Delta U'_{11}$  and  $\Delta U'_{10}$  decrease. Consequently, its value should be large enough only to ensure that  $\Delta U'_{00}$  is eliminated while  $\Delta U'_{11}$  and  $\Delta U'_{10}$  are maintained. Changing  $\varphi_{1x}$  adjusts the potential’s tilt with respect to the  $\varphi_1$  axis. If  $\varphi_{1x}$  takes on too large of a value, then the barrier  $\Delta U'_{01}$  will be undesirably eliminated. However, its value must be large enough to ensure that  $\Delta U'_{00}$  is eliminated. Similarly, tuning  $\varphi_{2x}$  changes the tilt of the potential with respect to the  $\varphi_2$  axis. If  $\varphi_{2x}$  is too large, then the blue (purple) stable (unstable) fixed points can annihilate, which causes information to be erased in the region where it should be preserved.

Obtaining effective circuit parameter ranges involves determining two particular values: (i) the value resulting in  $\Delta U'_{01}$ ,  $\Delta U'_{10}$ , and  $\Delta U'_{11}$  having the same height and (ii) the value which results in one barrier falling below the proxy line. The first (second) criterion serves as the lower (upper) ends of the range. Ultimately, there are clear tradeoffs that depend on the value of a given circuit parameter. Finding the set of parameters permitting control over which information is erased and preserved requires a balancing act: A careful process of selecting parameter values that are large enough to erase the desired information, but not so large that the information originally planned to be preserved ends up being erased.

For  $\mu$ , since  $\Delta U'_{11}$  is most susceptible to information leakage, its effective range corresponds to  $[0.06, 0.09]$ . Similarly, to maintain as large  $\Delta U'_{11}$  and  $\Delta U'_{10}$  as possible, the value of  $\varphi_{2\text{xdc}}$  should also lie at the lower end of the range  $[1.79, 1.88]$ . Then, to aid the effect of  $\mu$  and  $\varphi_{2\text{xdc}}$  on the potential and to maintain  $\Delta U'_{01}$ ,  $\varphi_{1x}$  would ideally take on a value within the range of  $[0.59, 0.65]$ . At the same time, to strike a balance between the increase of  $\Delta U'_{11}$  and the decrease of  $\Delta U'_{10}$ ,  $\varphi_{2x}$  ideally lies within the range  $[0.1, 0.15]$ . Within these ranges, a reliable CE can be performed.

### B. Control Erase Parameter Selection

We can now detail which circuit parameters—including their respective signs and magnitudes—are deployed for any of the eight CE protocols of interest. By leveraging the relationship between the potential’s dynamics and the circuit’s parameters, and the CE notation introduced in Sec. III, all eight CE protocols in Fig. 8 can be implemented in a systematic way. The following explains this

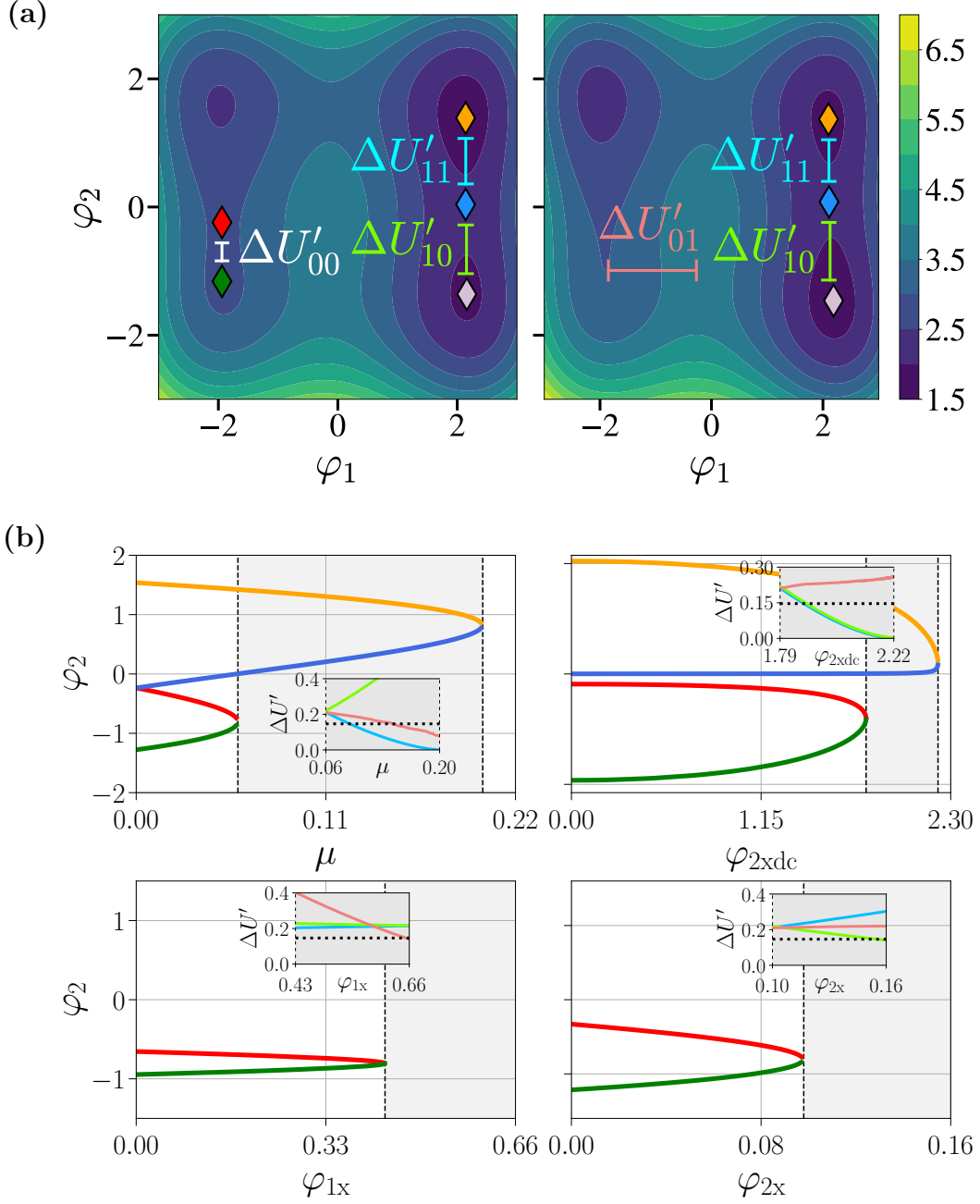


FIG. 5. Circuit parameter ranges that eliminate the dimensionless potential barriers  $\Delta U'_{00}$  and maintain  $\Delta U'_{11}$  and  $\Delta U'_{10}$ . In the insets, light blue, light green, and light red correspond to the barriers  $\Delta U'_{11}$ ,  $\Delta U'_{10}$  and  $\Delta U'_{01}$ , respectively. The barrier  $\Delta U'_{01}$  serves as the most conservative one for the 01 state during the CE. Last, the dotted line corresponds to a thermal energy barrier of  $50 k_B T$  at  $T = 100$  mK. (a) Specific fixed points (colored diamonds) within the potential energy landscape, as well as corresponding energy barriers, are utilized to investigate the CE in Fig. 2. (Left) Prior to the fixed point annihilation in the third quadrant. (Right) After fixed point annihilation that causes  $\Delta U'_{00}$  to vanish. Once all information stored in the 00 state is erased into the 01 state and the potential is subsequently brought back to its original configuration, the CE is completed. (b) Circuit parameter ranges for achieving the CE in Fig. 2, which can be accomplished by the annihilation of the green and red fixed points while maintaining the yellow and blue fixed points. Each circuit parameter range holds all other nonzero circuit parameters at the respective constant values:  $\mu = 0.06$ ,  $\varphi_{2\text{xdc}} = 1.79$ ,  $\varphi_{1x} = 0.59$ , and  $\varphi_{2x} = 0.10$ . These circuit parameters lead to effective CE protocols and thereby robust NAND gates.

approach, summarizing the results in Table II.

To begin, define a sign-based Iverson bracket:

$$[[P]] := \begin{cases} > 0 & \text{if } [P] = 1, \\ < 0 & \text{if } [P] = 0. \end{cases} \quad (4)$$

Here,  $[P]$  is the Iverson bracket of the statement  $P$ ;  $[P]$  evaluates to 1 if  $P$  is true, or 0 if  $P$  is false. This notation is useful when discussing how the sign of a circuit parameter is determined. Let's review the four parameters involved in each CE protocol:

- $\varphi_{ixdc}$  lowers the barrier between specific pairs of states to be erased;
- $\varphi_{jx}$  compensates for the unwanted effects of  $\varphi_{ixdc}$ ;
- $\mu$  biases the target erasure state to be more energetically favorable; and
- $\varphi_{ix}$  compensates for the unwanted effects of  $\mu$ .

For these parameters,  $i, j \in \{1, 2\}$  with  $i \neq j$ . To determine which  $\varphi_{ixdc}$  is utilized for a particular CE, recall that we specify a CE with three parameters:  $\rho$ ,  $\sigma$ , and  $A$ . If  $\rho = X$  ( $Y$ ), then  $i, j = 2, 1$  ( $1, 2$ ). As seen from Eq. (3),  $\varphi_{ixdc}$  appears only in the cosine function: Since this function is even, the sign of  $\varphi_{ixdc}$  is not relevant. Recall from Secs. III and V A that  $\varphi_{ixdc}$  lowers energy barriers on both sides of the  $i$ th axis, but the CE requires one barrier to be maintained. Thus, we need a control parameter to offset this barrier drop so that it applies to only one half of the  $\varphi_1$ - $\varphi_2$  plane, while maintaining the other barrier. The parameter deploying this barrier offset is  $\varphi_{jx}$ , and its sign is given by  $\llbracket \sigma \neq \rho \rrbracket$ .

Next,  $\mu$  biases the potential such that the minima along one of the diagonals of the  $\varphi_1$ - $\varphi_2$  plane are energetically favorable compared to those on the other diagonal. Its sign determines which well becomes the target for the erasure, and is given by  $\llbracket [\sigma = \rho] \text{ XOR } A \rrbracket$ . Recall that  $A \in \{0, 1\}$  is the state to which the control bit is erased. Since  $\mu$  acts along the diagonals of the plane, it has the unwanted effect of making both wells along a given diagonal more energetically favorable. This causes asymmetry between two wells that are supposed to be storing information, resulting unwanted information leakage. Fortunately, the parameter  $\varphi_{ix}$  can be used to compensate this effect by tilting the potential to offset this unintentional information leakage. The sign of this parameter is found through  $\llbracket A \rrbracket$ .

For all CEs of interest in Fig. 8, Table II compactly shows the signs of the relevant circuit parameters.

### C. CE Robustness

During our example CE in Fig. 5, once  $\Delta U'_{00}$  vanishes, the information needs to propagate from the 00 state to the 01 state. The time this takes is denoted  $t_{CE}$ ; it serves as a proxy for the CE timescale.

As this information is erased, other information is being stored in the 01, 10, and 11 states due to the barriers  $\Delta U'_{01}$ ,  $\Delta U'_{10}$ , and  $\Delta U'_{11}$  being maintained. However, we see in Fig. 5 that as a circuit parameter increases, at least one barrier's height decreases. The microstates stored in

these decreasing barriers are most susceptible to fluctuating out of their respective memory states. Due to this, the timescale that characterizes how long these states reliably store information is in competition with  $t_{CE}$ . This type of timescale is known as a dwell time [16, 18, 37], which is denoted  $t_d$ . Implicitly from Fig. 5, there are three dwell times that contribute to CE performance—those being the dwell times corresponding to the states 01, 10, and 11. The minimum of these three dwell times ultimately dictates CE failure.

If the length of time that information can be reliably stored is much longer than the timescale of a CE protocol, there is a low probability of error due to an unwanted thermally activated transition. To quantify this, we take the ratio  $t_d/t_{CE}$  as a measure of robustness.

To calculate  $t_{CE}$ , we approximate the information in the 00 state as a single damped particle travelling down a quadratic potential from the point where the fixed points initially annihilate; the derivation is included in App. A. For  $t_d$ , since there are three dwell times that affect CE performance, we choose the minimum of these dwell times to characterize CE robustness. This provides a more conservative estimate of a particular CE's performance; refer to App. B for details. From here, we note that the dwell time is exponentially proportional to  $L$  and  $T$ . This has a dominant effect on the robustness ratio  $t_d/t_{CE}$ . Therefore, studying the robustness as a function of  $L$  and  $T$  allows for interpreting the performance of a CE across the MQP and QFP literature.

From Sec. V A, selecting parameter values at the lower end of the effective parameter range yields a more robust CE: We found that  $\mu = 0.06$ ,  $\varphi_{ixdc} = 1.79$ ,  $\varphi_{ix} = 0.61$ , and  $\varphi_{jx} = 0.10$ . These will be known as the *effective parameter values*. With these, Fig. 6 displays the CE robustness for different values of  $L$  and  $T$ . Since the MQP (QFP) literature employ SQUIDs for different purposes—thereby leading to differing ranges of  $L$  and  $T$ —we separate the possible value ranges into the left (right) figures. The relevant MQP literature [16–19, 27, 29, 32, 33, 35, 38] corresponds to the left figure, which has a general temperature range of [100, 500] mK, while the inductance values range from [140, 300] pH. An upper value of  $\mathcal{O}(10^{48})$  CEs per device is obtained with the inductance value of  $L = 140$  pH found from Saira et al. [27] at  $T = 100$  mK.

On the right—corresponding to the QFP literature [4, 31, 39, 40]—the operating temperatures are no colder than 4.2 K, in addition to  $L \geq 10$  pH. To demonstrate robustness with a broader scope than constructed thus far, we use a range that begins at a theoretical value of  $L = 5$  pH to obtain an upper value of  $\mathcal{O}(10^{31})$  CEs per device at 4.2 K. For both areas of literature, we identify that lower temperature and inductance values correspond to a greater expected number of successful CEs per device. The values of  $R$ ,  $C$ , and  $I_c$  are chosen as typical values found in the respective literatures.

As a final point, note that from Fig. 6 the ratio  $t_d/t_{CE}$  was calculated with the effective parameter values. We

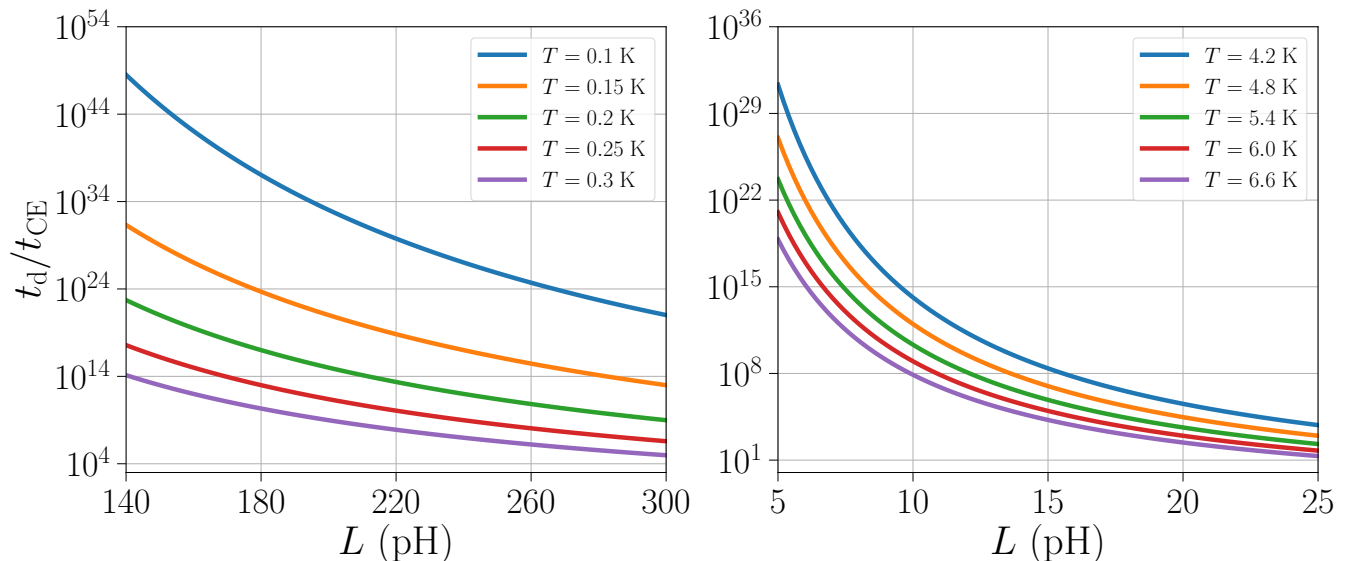


FIG. 6. The ratio  $t_d/t_{CE}$  characterizes the robustness of a particular device’s construction as an order of magnitude estimate. **(Left)** MQP literature inductance values and temperatures [16–19, 27, 29, 32, 33, 35, 38]. To demonstrate the behavior of the robustness at colder temperatures, the temperature range [100 – 300] mK is only displayed. Note that  $R = 1 \Omega$ ,  $C = 500 \text{ fF}$ , and  $I_c = 5 \mu\text{F}$ . **(Right)** QFP literature inductance and temperature values [4, 31, 39, 40]. Note that the values  $5 \leq L \leq 10 \text{ pH}$  are exercised to demonstrate the performance of a QFP if obtainable, while typical QFP inductances are greater than or equal to  $10 \text{ pH}$ . For this figure,  $R = 1 \Omega$ ,  $C = 1 \text{ pF}$  and  $I_c = 25 \mu\text{F}$ .

further assumed that the information travelling from the 00 state to the 01 state begins at the location determined from nonzero circuit parameters for the CE.

Now, suppose all circuit parameters were initialized to zero, so that the potential matches Fig. 1. Then, tune all circuit parameters infinitely fast to their respective final values. Due to this, the information stored in the 00 state is now travelling from the location determined by zero-valued circuit parameters, as opposed to the point of annihilation. Considering this scenario provides a more conservative estimate for the ratio  $t_d/t_{CE}$ , as the information from the 00 state must travel a greater distance to the 01 state, thereby resulting in a larger  $t_{CE}$ . However, this larger  $t_{CE}$  will be no more than twice the value of the most conservative estimate of  $t_{CE}$ , leading to a reduction of the robustness of order one compared to that shown in Fig. 6.

#### D. NAND Gate Application

Executing successive CE protocols allows for performing a NAND gate. The CE has two input bits and two output bits as seen from Fig. 3, while the NAND gate has two inputs but only one output bit. When the number of logical output bits is less than the number of embedded output bits in a computational system, there is added flexibility when choosing which bit to read as the output for a computation. For example, we can specify  $X' = \text{NAND}[X, Y]$  without prescribing the  $Y'$  computation. Thus, we define two kinds of NAND gates: a *par-*

*tial* NAND, written as  $P_{\rho'}[(X, Y)]$ , which only requires the state  $\rho'$  to yield the desired output, and a *complete* NAND, denoted as  $C[(X, Y)]$ , which requires that  $X' = Y' = \text{NAND}[X, Y]$ .

Fig. 7 illustrates both kinds of computation. Recall from Fig. 1 that the first, second, third, and fourth quadrants correspond to the memory states 11, 01, 00, and 10, respectively. In this example, carrying out only steps (1)-(3) executes the partial computation  $P_{Y'}$ . This can be seen by tracking the arrows through the included protocol steps: In step (1), the information in the state 10 is erased into the 00 state; in step (2), the combined information—comprising of the information from the initial 00 and 10 states—is erased into the 01 state; in step (3), the information in the 11 state is translated into the 10 state using the dynamics of the CE protocol. Note that in this step there is no logical erasure, since quadrant III was vacated in step (1). At this point, the  $Y'$  output bit represents a NAND gate of  $X$  and  $Y$ . Continuing to track the arrows for steps (4)-(5) completes computation  $C$ , assuming that  $X'$  also yields a NAND gate.

Partial NAND gates built from CEs require fewer successive CE protocol executions than complete NAND gates. However, performing complete NAND gates provides more redundancy regarding from which states the computations can be read.



(a)

$(X, Y)$	$\text{NAND}(X, Y)$	$P_Y(X, Y)$	$C(X, Y)$
00	1	01	11
01	1	01	11
10	1	01	11
11	0	10	00

(b)

(c)

Step	CE
1	$(C_{\bar{Y}}E_0, I_Y)$
2	$(I_X, C_{\bar{X}}E_1)$
3	$(I_X, C_XE_0)$
4	$(C_YE_1, I_Y)$
5	$(C_{\bar{Y}}E_0, I_Y)$

FIG. 7. NAND computations carried out on a coarse-grained potential of Fig. 1, which is reproducible by Eq. (3). (a) Tabulated computations of the NAND gate. Steps (1)-(3) execute the partial computation  $P_Y[(X, Y)]$ . Additionally, steps (1)-(5) accomplish the complete computation  $C[(X, Y)]$ . (b) Arrow-based schematic for performing partial and complete NAND gates. (c) Tabulated step numbers and CE protocols corresponding to Fig. (b).

## VI. CONCLUSION

We presented the family of control erase (CE) protocols in Fig. 8 and introduced notation in Sec. III that allows them to be concisely enumerated. We introduced a device in Fig. 4 that performs CE protocols by tuning circuit parameter values to access desired bifurcations. Characterizing a measure of a protocol’s robustness involved associating a storage length time with the protocol’s duration. We conducted an order of magnitude

estimate of the robustness for an example CE protocol in Fig. 6, yielding a high robustness for protocols that employ realistic parameter values spanning different areas of superconducting circuit literature.

Sec. VB established a connection between the device’s circuit parameters and the CE notation. Linking various CE protocols together by leveraging this relationship allowed for universal computations. Sec. VD demonstrated a NAND gate that employs only CEs. Due to its superconducting operation, the device performs CE-based universal computations at extremely low energy cost.

In addition, there is added flexibility when performing NAND gates via the potential in Fig. 1. Partial computations permit fewer executions of erasure protocols, which implies that computations can be performed with even lower energetic costs. Conversely, executing complete computations gives rise to reading the same computation regardless of which axis is chosen to be the output, thereby providing an added layer of redundancy.

Follow-on efforts explore the thermodynamic efficiency of this NAND gate, SPICE simulations of the protocol for varying circuit constructions, and investigations into implementing other useful and more complex logical operations.

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\* czpratt@ucdavis.edu

† kjray@ucdavis.edu

‡ chaos@ucdavis.edu

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### Appendix A: Control Erase Timescale Approximation Scheme

In this section, we detail an approximation scheme for the potential in Eq. (3) during the control erase (CE) protocol described in Sec III. Specifically, to represent the distribution of microstates being erased into the 01 state, we approximate this situation as a particle rolling down a quadratic slope. From this, we calculate  $t_{CE}$ —

Circuit quantity	$z'(z_c)$	Identifications
$m$		$m'(C)$
$\gamma$		$\gamma'(1/R)$
$\phi$		$\varphi(\phi_c)$
$U$		$U'(\phi_c^2/L)$
$t$		$t'(\sqrt{LC})$

TABLE I. Relevant circuit quantity scalings.

the time it takes for the particle to travel to the bottom of the slope.

First, note that in Fig. 3, the coordinate  $\phi_1$  has negligible change in comparison to the change in  $\phi_2$ . With this in mind, we will consider the potential to be dependent only on  $\phi_2$ . Next, the height of the potential  $U$  that the particle travels down is on the order of  $U_0 \sim 10^{-22}$ : Essentially, the particle's motion can be described in terms of  $\phi_2$  without loss of generality. Then, there are two forces acting on the particle: (i) the force due to the potential  $-dU/d\phi_2$ , and (ii) the classical damping force  $-\gamma d\phi_2/dt$ . This means that the particle's motion is described by Newtonian mechanics due to the influence of a dimension-full potential  $U$  and damping coefficient  $\gamma$ , written as:

$$\frac{d^2\phi_2}{dt^2} + \frac{\gamma}{m} \frac{d\phi_2}{dt} + \frac{1}{m} \frac{dU}{d\phi_2} = 0. \quad (\text{A1})$$

First, we note that Eq. (3) is dimensionless, while Eq. (A1) describes a particle's motion under the influence of a potential with units of energy. To reconcile this, we must rewrite Eq. (A1) in terms of dimensionless quantities. Ref. [35] detailed a strategy for converting dimension-full equations of motion—such as Eq. (A1)—into dimensionless equations of motion. To do this, we write a dimensional quantity  $z$  as  $z = z'z_c$  in which  $z'$  is the dimensionless representation of the quantity, while  $z_c$  represents a dimensional scaling factor: Table I summarizes the circuit quantity scaling parameters  $z_c$ .

Now, after appropriately making substitutions and simplifying, we write the dimensionless Eq. (A1) as:

$$\frac{d^2\varphi_2}{dt'^2} + \Lambda \frac{d\varphi_2}{dt'} + \theta \frac{dU'}{d\varphi_2} = 0, \quad (\text{A2})$$

where  $\Lambda = \gamma'\sqrt{LC}/m'RC$  and  $\theta = 1/m'$ .

The approximation scheme of the potential will now be detailed. First, we write the dimension-full potential as  $U(\phi_2) = k\phi_2^2/2$ , where  $k$  now serves as the ‘spring constant’ of the potential. In dimensionless form, the potential reads:  $U'(\varphi_2) = k'\varphi_2^2/2$ . This implies that  $k_c = U_c/2\phi_c^2$ , and furthermore  $k' = U'/(\varphi_2)^2$ . Now, the particle's motion is written as:

$$\frac{d^2\varphi_2}{dt'^2} + 2\lambda \frac{d\varphi_2}{dt'} + \omega^2\varphi_2 = 0, \quad (\text{A3})$$

which is analogous to the differential equation modelling a damped harmonic oscillator which oscillates at frequency  $\omega^2 = k'\theta$  under damping coefficient  $\lambda = \Lambda/2$ . We deploy the ansatz:  $\varphi_2(t) = Ae^{\alpha t}$  in which  $\alpha = -\lambda \pm \sqrt{\lambda^2 - \omega^2} = -\lambda \pm \Omega$ . Depending on the value of  $R$ ,  $L$  and  $C$ ,  $\Omega > 0$  or  $\Omega < 0$ : These two situations will be categorized as ‘overdamped’ and ‘underdamped’, respectively, in the subsequent discussion.

#### a. Overdamped

When  $\Omega > 0$ , the solution to Eq. (A3) is [41]:

$$\varphi_2(t') = A \exp(-(\lambda - \Omega)t') + B \exp(-(\lambda + \Omega)t'), \quad (\text{A4})$$

which describes an overdamped oscillator with initial conditions  $A$  and  $B$ . To understand them, we first detail the consequences of the particle-like representation of the distribution of microstates. The average position of this distribution localizes to a position at any given time—represented by a particle in this case—while its average initial velocity will be zero. With this, the initial conditions are (i)  $\varphi_2(t' = 0) = \varphi_2^o$ , and (ii)  $d\varphi_2(t' = 0)/dt' = 0$ . Solving for these two initial conditions, and substituting the results back into Eq. (A4) gives:

$$\varphi_2(t') = \frac{\varphi_2^o}{\Omega} (\lambda + \Omega) e^{-\lambda t'} \sinh(\Omega t') + \varphi_2^o e^{-(\lambda + \Omega)t'}. \quad (\text{A5})$$

Numerically solving Eq (A5) for a final time  $t' = t'_f$ , and multiplying the result by  $\sqrt{LC}$ , yields  $t_{\text{CE}} = t'_f \sqrt{LC}$ .

#### b. Underdamped

If  $\Omega < 0$ , we must define  $\tilde{\omega} = \sqrt{\omega^2 - \lambda^2}$  in order for the general solution to be written as [41]:

$$\varphi_2(t') = D \exp(-\lambda t') \cos(\tilde{\omega} t' + \theta). \quad (\text{A6})$$

Eq. (A6) describes an underdamped harmonic oscillator for which the coefficient  $D$  and phase  $\theta$  are solved using initial conditions. Subsequently solving for them in the same manner as before, and substituting the results into Eq. (A6), produces:

$$\varphi_2(t') = \varphi_2^o \sqrt{1 + \left(\frac{\lambda}{\tilde{\omega}}\right)^2} \exp(-\lambda t') \cos(\tilde{\omega} t' + \Theta),$$

for which  $\Theta = \arctan(\lambda/\tilde{\omega})$ .

## Appendix B: Dwell Time

The escape rate [27, 42, 43] in the  $l = 1, 2$  direction is:

$$\Gamma_l = \frac{\omega_{p,l}}{2\pi} \exp\left(-\frac{\Delta U_b}{k_B T}\right). \quad (\text{B1})$$

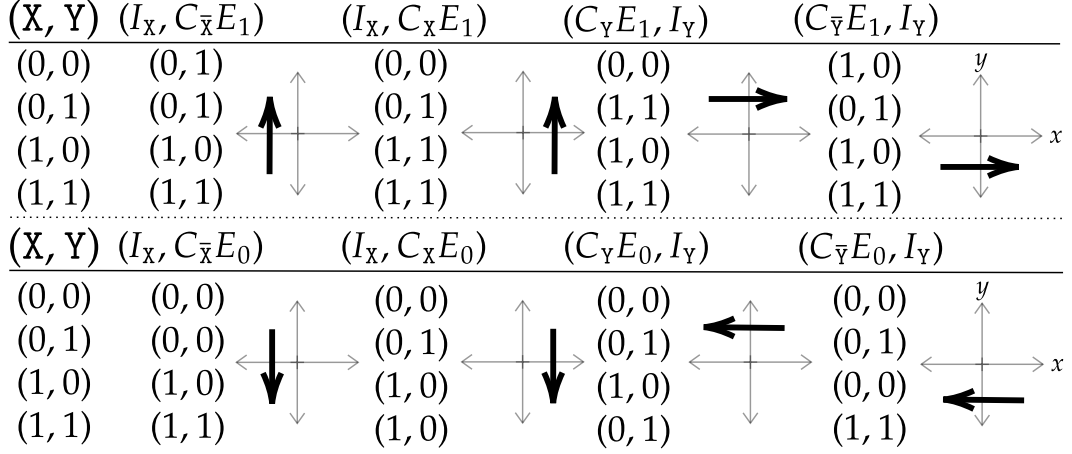


FIG. 8. All control erasure protocols of interest for this work, displayed with arrow-based notation first shown in Fig. 3.

First,  $\omega_{p,l}$  is the plasma frequency in the  $l$ th flux direction. To understand it, we consider the dimension-full potential  $U(\phi_1, \phi_2)$ , perform a Taylor expansion around a minimum ( $\phi_1 = \phi_1^*, \phi_2 = \phi_2^*$ ), and only look to the second order terms whose partial derivatives are both either with respect to  $\phi_1$  or  $\phi_2$ :

$$U(\phi_1^*, \phi_2^*) \sim \frac{1}{2} \left. \frac{\partial^2 U}{\partial \phi_1^2} \right|_{(\phi_1^*, \phi_2^*)} (\phi_1 - \phi_1^*)^2 + \frac{1}{2} \left. \frac{\partial^2 U}{\partial \phi_2^2} \right|_{(\phi_1^*, \phi_2^*)} (\phi_2 - \phi_2^*)^2.$$

We identify that a partial derivative taken with respect to  $\phi_l$ , and subsequently evaluated at the minimum, corresponds the spring constant  $k_l$ . From here, we take the corresponding plasma frequency to be  $\omega_l = \sqrt{k_l/m}$  for which the dimension-full mass  $m = C$ .

Furthermore,  $\Delta U_b$  indicates the barrier height between a local minima and a local maxima;  $k_B$  is the Boltzmann constant; and  $T$  is the circuit's operating temperature.  $\Gamma_l$  characterizes how many escape events are expected out of the minima per second. Finally, the dwell time is the reciprocal of Eq. (B1):  $t_{d,l} = 1/\Gamma_l$ . Explicitly, the plasma frequencies of interest for the dimensionless

barriers  $\Delta U'_{01}$  ( $\Delta U'_{11}$  and  $\Delta U'_{10}$ ) correspond to the flux direction  $l = 1$  ( $l = 2$ ). Then, for values of  $L$  and  $T$  in Fig. 6, we select the minimum dwell time to calculate the robustness  $t_d/t_{CE}$ .

### Appendix C: Control Erasures of Interest

Fig. 8 exhibits all control erasure protocols of interest. Successive executions of a subset of these protocols can lead to performing a NAND gate. Note that this is not an exhaustive illustration of possible control erasure protocols, but only represent those of this work's interest. Table II shows the indices, signs and relationships of the relevant circuit parameters for a particular CE. In the notation of Sec. VB, the non-zero barrier-control parameter is determined by  $j$ . Meanwhile, the magnitudes of the tilt parameters which offset the bias and barrier changes to the potential are related by  $|\varphi_{ix}| > |\varphi_{jx}|$ , respectively. By using the effective magnitudes of the circuit parameters detailed in Sec. VC and successively executing effective CE protocols, a robust NAND gate can be performed.

	$(I_X, C_{\bar{X}}E_1)$	$(I_X, C_XE_1)$	$(C_YE_1, I_Y)$	$(C_{\bar{Y}}E_1, I_Y)$	$(I_X, C_{\bar{X}}E_0)$	$(I_X, C_XE_0)$	$(C_YE_0, I_Y)$	$(C_{\bar{Y}}E_0, I_Y)$
$i$	1	1	2	2	1	1	2	2
$j$	2	2	1	1	2	2	1	1
$\text{sgn}(\varphi_{1x})$	+	-	+	+	+	-	-	-
$\text{sgn}(\varphi_{2x})$	+	+	-	+	-	-	-	+
$\text{sgn}(\mu)$	+	-	-	+	-	+	+	-

TABLE II. Tabulated summary of the relationship between experimental circuit parameters—including their indices and signs—and the CE notation introduced in Sec. III. Here, + (-) corresponds to the sign of a particular circuit parameter, that being  $> 0$  ( $< 0$ ). Note that the non-zero barrier flux control parameter for a given CE is determined by  $j$ . Meanwhile, the magnitudes of the tilt parameters—which offset the bias (barrier) effect of  $\mu$  ( $\varphi_{j\text{dc}}$ )—are related by  $|\varphi_{ix}| > |\varphi_{jx}|$ , respectively.